
HIGH PERFORMANCE MIDI SYNTH AND EFFECT PROCESSOR

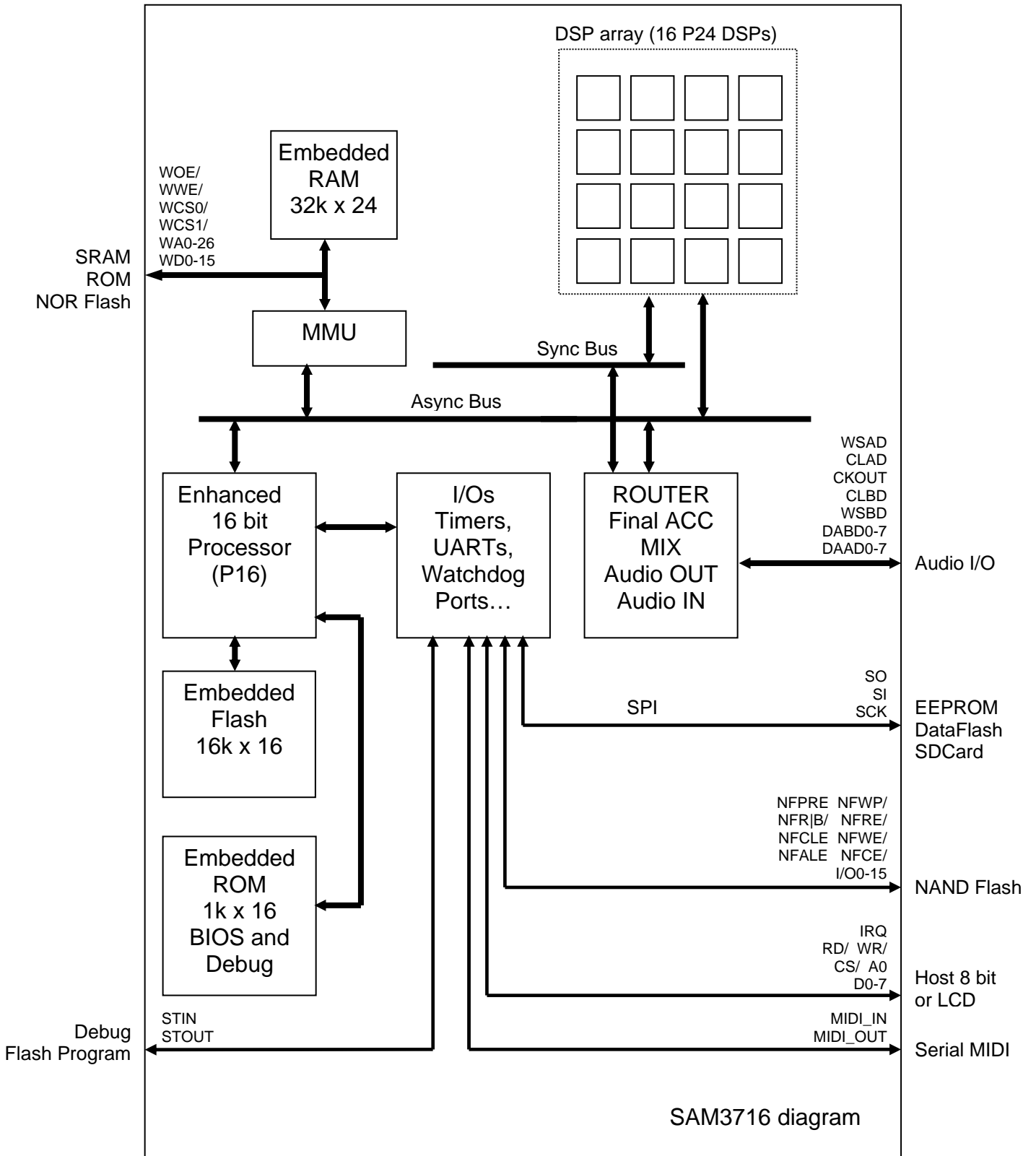
Key features

- ❑ up to 126 voices high quality Sound Synthesis
- ❑ additional professional Effects: Reverb, Chorus, Delay, Equalizer etc.
- ❑ additional compressed Audio Player (MP3, MP2) possible
- ❑ maximum single shot PCM wave size of 16M samples
- ❑ external memory up to 2 x 256 MegaBytes
- ❑ various high quality sound sets available
- ❑ wide library of sound effects available
- ❑ up to 16 audio channels in, 16 audio channels out
- ❑ serial interface / MIDI IN/OUT
- ❑ 4 programmable memory chip selects
- ❑ SPI (mode 0) interface for Dataflash, EEPROM, or SD-Card
- ❑ numerous Multi-function pins
 - up to 5 alternate functions per pin
 - up to 60 General Purpose I/O pin
- ❑ 8-bit parallel Host Port
- ❑ 16 DSP's with double precision instructions and enhanced Audio routing
- ❑ new P16 with optimized instructions for C compiler
- ❑ built in RAM 32k x 24
- ❑ built in Flash 16k x 16 for resident firmware and Code protection
- ❑ Watchdog
- ❑ deep Power Down
- ❑ 128-pin LQFP package

Typical applications

- ❑ High end sound module
- ❑ Karaoke
- ❑ Crossover, Speaker Management
- ❑ Multi Effect Devices

1. SAM3716 Internal Architecture



The SAM3716 is a new member of the SAM3000 family of sound synthesis/processing ICs that uses the DSP array technology.

The SAM3716 includes sixteen 24-bit DSPs, a 24-bit Audio Router and a general-purpose 16-bit processor with new instructions and a C compiler for quicker reliable firmware development. Its high performance and flexibility with 16-input/16-output channels enables implementation of multi-task audio applications in gaming or karaoke products, such as multiple MP3 decoding with time stretch and pitch control, concurrent Wavetable synthesis and, effect processing and digital mixing. A variety of I/Os, including external Wave ROM, NAND Flash and DataFlash® are provided. Sampling rates up to 144 kHz at 24 bits are supported.

- DSP Array

The SAM3716 includes 16 on-chip DSPs.

Each DSP (P24) is built around a 2k x 24 RAM and a 1.2k x 24 ROM. The RAM contains both data and P24 instructions; the ROM contains typical coefficients such as FFT cosines and windowing. A P24 sends and receives audio samples through the Sync Bus. It can request external data such as compressed audio through the Async Bus. Each P24 RAM can be accessed through the Async Bus.

Each P24 is capable of typical MAC operation loops, including auto-indexing, bit reverse and butterfly (multiplication of complex numbers). It also includes specialized audio instructions such as state variable IIR filtering, envelope generation, linear interpolation and wavetable loop. The DSP's have new 48-bit double precision instructions for improved Pro Audio applications.

One P24 is sufficient for processing one channel MPEG1 Layer2, implementing a multi-tap delay line or a multi-tap transversal filter.

- Sync Bus

The Sync Bus transfers data on a frame basis, typical frame rates being 32, 44.1, 48, 96 kHz. Each frame is divided into 32 time slots. Each slot is divided into 8 bus cycles. Each P24 is assigned a hardwired time slot (16 to 31), during which it may provide 24-bit data to the bus (up to 8 data samples). Each P24 can read data on the bus at any time, allowing inter P24 communication at the current sampling rate. Slots 0 to 15 are reserved for a specific router DSP, which also handles audio out, audio in, and remix send.

- Async Bus

The Async Bus is 24-bit data inside the chip and 16-bit outside.

The P16 processor normally masters the Async Bus, it can read/write the P24 memories and the external ROM/RAM or embedded RAM. However, each P24 can request a bus master cycle for accessing external ROM/RAM or other P24 memories. This allows efficient intercommunication between several P24s on asynchronous block basis. Specific P24 instructions FLOAT and FIX allow to convert fixed point DSP data to floating point 16 bits. This allows for 20-bit audio dynamic range when using 16-bit external memory.

- Enhanced 16-bit processor

This is the new enhanced version of P16 processor with added instructions allowing optimized use of C compiler. Using the P16, widely used in Dream products, maintains continuity for the large firmware investments from the SAM97xx series. A built-in Flash is connected to the P16 to allow fast code fetch. The P16 ROM holds basic input/output software (BIOS) for peripherals such as UART, DataFlash®, as well as a debugger which uses a dedicated asynchronous serial line, or interface with host processor through a 8-bit parallel port. The firmware can reside on the built-in 16k x 16 Flash or it can be downloaded at power-up into the built-in 32k x 24 RAM from host.

- MMU (memory management unit)

The MMU handles transfer requests between the external memories (SRAM, NOR Flash, ROM) or embedded RAM, the P16 and the P24s through the Async Bus. The SAM3716 includes an on chip 32k x 24 RAM.

- Router: final ACC, MIX, audio out, audio in

This block includes a RAM, accessed through the Async Bus, which defines the routing from the Sync Bus to/from the Audio I/O or back to the Sync Bus (mix send). It takes care of mix and accumulation from Sync Bus samples. 16 channels of audio in and 16 channels of audio out are provided (8 stereo in/out, I2S or MSB Left format). The stereo audio in channels may have a different sampling rate than the audio out channels. In this case, one or more P24s take care of sampling rate conversion.

- I/O

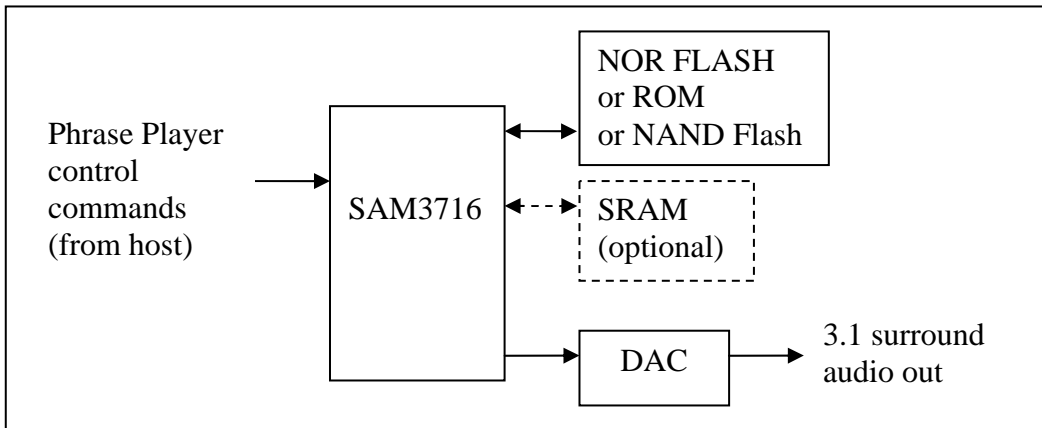
The SAM3716 includes very versatile I/Os, that share common pins for reduced pin count and small IC footprint. Most I/Os, when not used for a specific function, remain available as firmware controlled general-purpose pins.

The following peripherals are included on chip:

- 2 x 8-bit timers
- 2 x 16-bit timers
- Parallel slave 8-bit port, MPU401 compatible
- Parallel master 8-bit port, for connection to NAND flash, /or LCD display, switches, etc.
- 2 x asynchronous bi-directional serial port (one used as debug interface).
- Synchronous serial slave port (SPI type host connection).
- Firmware controlled I/O pins.

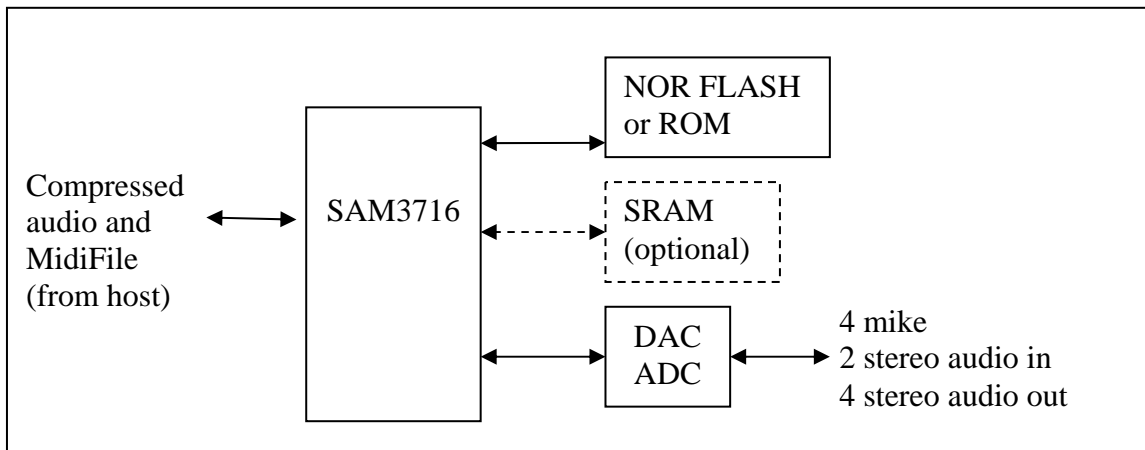
2. Typical application examples

2.1. Gaming



- Up to 16 compressed Audio Phrase Players (enhanced MPEG1 Layer2 format)
- MIDI synthesis
 - Up to 126 voices with effects (reverb, chorus,...) @ 48kHz sampling rate
 - Legendary Dream high quality wavetable sound
- Choice of host communication interfaces:
 - 8-bit parallel
 - Asynchronous serial (MIDI)
 - Synchronous serial (SPI)
- Built-in Standard Midi file player (SMF) dramatically reduces host load

2.2. Karaoke



- Stereo MP3 stream via 8-bit parallel port
- Full MP3 support including very low bit rates extension (ISO/IEC 13818-3)
- Easily upgradable to other coding standards
- MIDI synthesis
 - Up to 126 voices with effects (reverb, chorus,...) @ 48kHz sampling rate
 - Legendary Dream high quality wavetable sound
- Choice of host communication interfaces:
 - 8-bit parallel
 - Asynchronous serial (MIDI)
 - Synchronous serial (SPI)
- Built-in Standard Midi file player (SMF) dramatically reduces host load

3. SAM3716 capacity and I/O configuration

The SAM3716 can run firmware directly from an embedded Flash memory or from an external ROM/Flash/SRAM memory. It may also run firmware from local RAM. The SAM3716 is the ideal choice when high DSP power, external components low count and many I/O pins are required.

3.1. DSP considerations

The SAM3716 includes 16 x P24 DSPs.

The table below lists the performance achievable by the P24:

Function	P24s required
MPEG1 Layer2 single track decode	1
MPEG1 Layer3 (MP3) decode (stereo)	3
9-voice wavetable synthesis @48kHz	1
Stereo reverb and chorus @48kHz	1
Stereo 10-band equalizer @48kHz	1
Stereo 31-band equalizer @48kHz	3

3.2. I/O selection considerations

I/Os are organized in groups, which can be mutually exclusive because they share the same IC pins (please refer to the pinout to identify the exclusions). The two main types of operation are host controlled and stand-alone.

3.2.1. Host-controlled operation

There are 3 main ways of communication with a host processor:

- 8-bit parallel MPU type bi-directional interface
signals: D7-D0, CS/, WR/, RD/, A0, IRQ
- Asynchronous serial, MIDI_IN and MIDI_OUT
- Synchronous serial
signals: SDIN, SCLK, SYNC, INT/

3.2.2. Stand-alone operation

Possible stand-alone modes are:

- Firmware into built in Flash memory
- Firmware into built in Flash memory plus firmware extension in external memory.

4. SAM3716 PINOUT

4.1. Pin description

Identical sharing number indicates multifunction pins.

Pd indicates pin with built-in pull-down resistor. (Pd) indicates that the pull-down can be disabled.

Pu indicates pin with built-in pull-up resistor. (Pu) indicates that the pull-down can be disabled.

_{5VT} indicates a 5 volt tolerant Input or I/O pin.

MEM indicates a pad supplied by VM33.

Pin name	Pin#	Type	Sha ring	Description
GND	5,12,23,33,45,54,78,100,106,108,111,119,	PWR	-	Digital ground. All these pins should be returned to a ground plane
VD18	104	PWR	-	Power for the internal PLL, +1.8V nominal (1.8V ± 10 %). These pins can be connected to the output of the regulator OUTVC182 (pin 46). A 100nF decoupling capacitor should be connected between this pin and PLL ground (pin100).
VD33	47,77,107,109	PWR	-	+3.3V power for internal 3.3V to 1.8 V regulators and periphery. All these pins should be returned to nominal 3.3V.
VM33	11,24,38,114,127	PWR	-	Memory PAD Power +2.25V to +3.6V. All VM33 pins should be returned to 3.3V
OUTVC181, OUTVC182	110,46	PWR	-	3.3V to 1.8 V regulator outputs. The 2 built-in regulators give 1.8V for internal use (core supply). PLL supply pin VD18 could also be connected to OUTVC182. Decoupling capacitors 470pF in parallel with 2.2 or 4.7µF must be connected between each OUTVC18x pin and GND
VREF	10	In	-	VM33/2 reference for memory pads.
D0-D7	75,74,73,72,71,70,69,68	I/O _{5VT} (Pd)	1	Slave 8-bit interface data. Output if CS/ and RD/ are low (read from chip), input if CS/ and WR/ are low (write to chip). Type of data defined by A0 input.
I/O7-I/O0	75,74,73,72,71,70,69,68	I/O _{5VT} (Pd)	1	NAND flash data or other peripheral data
P0.7-P0.0	75,74,73,72,71,70,69,68	I/O _{5VT} (Pd)	1	General purpose I/O can individually be programmed as input or output
A0	79	In _{5VT} (Pu)	2	Slave 8-bit interface address. Indicates data/status or data/ctrl transfer type (CS/ RD/ low or CS/ WR/ low)
SCLK	79	In _{5VT} (Pu)	2	Serial slave synchronous interface input clock
NFPRE	79	Out	2	NAND Flash Power-on Read Enable
P0.10	79	I/O _{5VT} (Pu)	2	General purpose I/O pin
CS/	82	In _{5VT} (Pu)	3	Slave 8-bit interface chip select, active low.
SYNC	82	In _{5VT} (Pu)	3	Serial slave synchronous interface input sync signal
P0.11	82	I/O _{5VT} (Pu)	3	General purpose I/O pin
WR/	80	In _{5VT} (Pu)	4	Slave 8-bit interface write, active low. D7-D0 data is sampled by chip on WR/ rising edge if CS/ is low
NFWP/	80	OUT	4	NAND Flash Write Protect, active low
P0.12	80	I/O _{5VT} (Pu)	4	General purpose I/O pin

RD/	81	In _{5VT} (Pu)	5	Slave 8-bit interface read, active low. D7-D0 data is output when RD/ goes low and CS/ is low
NFR B/	81	In _{5VT} (Pu)	5	NAND Flash Ready Busy/ status
P0.13	81	I/O _{5VT} (Pu)	5	General purpose I/O pin
MIDI_IN	83	In _{5VT} Pu	6	Serial MIDI in
SDIN	83	In _{5VT} Pu	6	Serial slave synchronous interface input data
P0.14	83	In _{5VT} Pu	6	General purpose input pin
IRQ	76	Out	7	Slave 8-bit interface interrupt request. High when data is ready to be transferred from chip to host. Reset by a read from host (CS/=0 and RD/=0)
INT/	76	Out	7	Serial slave synchronous interface data request, active low.
NFRE/	76	Out	7	NAND Flash Read Enable, active low
P0.8	76	I/O _{5VT}	7	General purpose I/O pin
MIDI_OUT	84	Out	8	Serial MIDI out
P0.9	84	I/O _{5VT}	8	General purpose I/O pin
DABD0	90	Out		Stereo channel 0 of digital audio output, I2S or MSB format
DABD1	48	Out	9	Stereo channel 1 of digital audio output, I2S or MSB format
NFWP/	48	Out	9	NAND Flash Write Protect, active low
P2.8	48	I/O _{5VT}	9	General purpose I/O pin
DABD2	49	Out	10	Stereo channel 2 of digital audio output, I2S or MSB format
NFR B/	49	In _{5VT}	10	NAND Flash Ready Busy/ status
P2.9	49	I/O _{5VT}	10	General purpose I/O pin
DABD3	50	Out	11	Stereo channel 3 of digital audio output, I2S or MSB format
NFRE/	50	Out	11	NAND Flash Read Enable, active low
P2.10	50	I/O _{5VT}	11	General purpose I/O pin
DABD4	51	Out	12	Stereo channel 4 of digital audio output, I2S or MSB format
NFCLE	51	Out	12	NAND Flash Command Latch Enable
P2.11	51	I/O _{5VT}	12	General purpose I/O pin
DABD5	52	Out	13	Stereo channel 5 of digital audio output, I2S or MSB format
NFWE/	52	Out	13	NAND Flash Write Enable, active low
P2.12	52	I/O _{5VT}	13	General purpose I/O pin
DABD6	53	Out	14	Stereo channel 6 of digital audio output, I2S or MSB format
NFALE	53	Out	14	NAND Flash Address Latch Enable
P2.13	53	I/O _{5VT}	14	General purpose I/O pin
DABD7	55	Out	15	Stereo channel 7 of digital audio output, I2S or MSB format
NFCE/	55	Out	15	NAND Flash Chip Enable, active low
P2.14	55	I/O _{5VT}	15	General purpose I/O pin
DAAD6, DAAD7	62,63	In _{5VT} (Pd)	16	Stereo audio data inputs, I2S or MSB format. Can operate on CLBD master rate or CLAD external rate when sampling rate conversion is requested.
I/O6,I/O7	62,63	I/O _{5VT} (Pd)	16	NAND flash data or other peripheral data
P2.6,P2.7	62,63	I/O _{5VT} (Pd)	16	General purpose I/O pins
WSADX1, CLADX1	62,63	In _{5VT} (Pd)	16	Optional word select and bit clock for digital audio inputs. DAAD0 and/or DAAD1, ..., DAAD7. Used for sampling rate conversion, for external incoming digital audio such as AES/EBU or S/PDIF.

DAAD4, DAAD5	60,61	In _{5VT} (Pd)	17	Stereo audio data inputs, I2S or MSB format. Can operate on CLBD master rate or CLAD external rate when sampling rate conversion is requested.
I/O4,I/O4	60,61	I/O _{5VT} (Pd)	17	NAND flash data or other peripheral data
P2.4,P2.5	60,61	I/O _{5VT} (Pd)	17	General purpose I/O pins
WSADX2, CLADX2	60,61	In _{5VT} (Pd)	17	Optional word select and bit clock for digital audio inputs DAAD0 and/or DAAD1.
DAAD0 – DAAD3	56-59	In _{5VT} (Pd)	18	Stereo audio data inputs, I2S or MSB format. Can operate on CLBD master rate or CLAD external rate when sampling rate conversion is requested.
I/O0 - I/O3	56-59	I/O _{5VT} (Pd)	18	NAND flash data or other peripheral data
P2.0 - P2.3	56-59	I/O _{5VT} (Pd)	18	General purpose I/O pins
WSAD	66	In _{5VT} (Pd)	19	Optional word select for all digital audio inputs. Used for sampling rate conversion, for external incoming digital audio such as AES/EBU or S/PDIF.
P3.8	66	I/O _{5VT} (Pd)	19	General purpose I/O pin
CLAD	65	In _{5VT} (Pd)	20	Optional bit clock for all digital audio inputs. Used for sampling rate conversion, for external incoming digital audio such as AES/EBU or S/PDIF.
P3.9	65	I/O _{5VT} (Pd)	20	General purpose I/O pin
CLBD	88	Out	-	Audio bit clock for DABD7-1. Audio bit clock for DAAD7-0 if CLAD is not used.
WSBD	89	Out	-	Audio left/right channel select for DABD7-0. Audio left/right channel for DAAD7-0 if WSAD is not used.
CKOUT	87	Out	-	External DAC/Codec master clock. Can be programmed to be 128x F_s , 192x F_s , 256x F_s , 384x F_s , 512x F_s , F_s being the DAC/Codec sampling rate.
WA26	44	Out MEM	21	External memory address bit, extension to 2 Gbits
NFCE/	44	Out MEM	21	NAND Flash Chip Enable, active low
XCS23/	44	Out MEM	21	Programmable Extended chip select for 2 nd memory device in 2-device mode or 3 rd memory device in 4-device mode.
P1.11	44	I/O MEM	21	General purpose I/O pin
WA25	43	Out MEM	22	External memory address bit, extension to 1 Gbits
NFALE	43	Out MEM	22	NAND Flash Address Latch Enable
XCS04/	43	Out MEM	22	Programmable Extended chip select for 4 th memory device in 4-device mode.
P1.10	43	I/O MEM	22	General purpose I/O pin
WA24	42	Out MEM	23	External memory address bit, extension to 512 Mbits
NFRE/	42	Out MEM	23	NAND Flash Write Enable, active low
XCS02/	42	Out MEM	23	Programmable Extended chip select for 2 nd memory device in 4-device mode.
P1.9	42	I/O MEM	23	General purpose I/O pin
WA23	41	Out MEM	24	External memory address bit, extension to 256 Mbits
NFCLE	41	Out MEM	24	NAND Flash Command Latch Enable
P1.8	41	I/O MEM	24	General purpose I/O pin
WA22	40	Out MEM	25	External memory address bit, extension to 128 Mbits
NFRE/	40	Out MEM	25	NAND Flash Read Enable, active low
P1.7	40	I/O MEM	25	General purpose I/O pin
WA21	39	Out	26	External memory address bit, extension to 64 Mbits
NFR B/	39	In MEM	26	NAND Flash Ready Busy/ status
P1.6	39	I/O MEM	26	General purpose I/O pin

WA20	37	Out MEM	26	External memory address bit, extension to 32 Mbits
NFWP/	37	Out MEM	26	NAND Flash Write Protect, active low
P1.5	37	I/O MEM	26	General purpose I/O pin
WA19	36	Out MEM	27	External memory address bit, extension to 16 Mbits
NFPRE	36	Out MEM	27	NAND Flash Power-on Read Enable
P1.4	36	I/O MEM	27	General purpose I/O pin
WA18	35	Out MEM	28	External memory address bit, extension to 8 Mbits
FS1	35	In MEM	28	Freq sense, sensed at power up. FS1 FS0 allow firmware to know operating freq of chip as follows (optional): 00- 12 MHz 01- 9.6 MHz 10- 11.2896 MHz 11- 12.288 MHz
P1.3	35	I/O MEM	28	General purpose I/O pin
WA17	34	Out MEM	29	External memory address bit, extension to 4 Mbits
FS0	34	In MEM	29	Freq sense, sensed at power up. Together with FS1, allows the firmware to know the operating freq of the chip (see FS1)
P1.2	34	I/O MEM	29	General purpose I/O pin
WA15, WA16	30,31	Out MEM	30	External memory address bits, extension to 1 and 2 Mbits
P1.0,P1.1	30,31	I/O MEM	30	General purpose I/O pins
WA0 – WA14	13-22,25-29,	Out MEM	-	External memory address bits, up to 512 kbits (32k x 16)
WD0-WD15	117,118,120-126,2-4,6-9	I/O MEM	31	External memory data
I/O0-I/O15	117,118,120-126,2-4,6-9	I/O MEM	31	NAND Flash data or other peripheral data
P4.0-P4.15	117,118,120-126,2-4,6-9	I/O MEM	31	General purpose I/O pins
WCS1/	116	Out MEM	-	External memory chip select 1, active low. Pre-decode for an external RAM/Flash/ROM.
WCS0/	115	Out MEM	32	External memory chip select 2, active low. Pre-decode for an external RAM/Flash/ROM. When using more than one memory device, Extended Chip Select XCS11, XCS23, XCS02 and XCS04 can be used instead of WCS0/
XCS11/	115	Out MEM	32	Programmable Extended chip select for 1 st memory device in 2-device mode or 1 st memory device in 4-device mode.
WOE/	112	Out MEM	-	External memory output enable, active low.
WWE/	113	Out MEM	-	External memory write enable, active low.
DFSI	91	Out	-	DataFlash serial input (to DataFlash)
DFSO	92	In 5VT Pd	-	DataFlash serial output (from DataFlash). This pin has a built-in pull-down. It may be left open if not used.
DFSCK	93	Out	-	DataFlash data clock
X1,X2	101,102	-	-	External crystal connection. Standard frequencies are 12 MHz, 9.6 MHz, 11.2896 MHz, 12.288 MHz. Max frequency is 12.5 MHz. An external clock (max. 1.8Vpp) can be connected to X1 using AC coupling (22pF). A built-in PLL multiplies the clock frequency by 4 or by 6 for internal use. No external compensation capacitors are needed.
LFT	103	-	-	PLL decoupling RCR filter.
RESET/	94	In 5VT	-	Master reset Schmitt trigger input, active low. RESET/ should be held low during at least 10ms after power is applied. On the rising edge of RESET/, the chip enters an initialization routine, which may involve firmware download from a host.
STIN	85	In 5VT Pd	-	Serial test input. This is a 57.6 kbauds asynchronous input used for firmware debugging. This pin is tested at power-up. The built-in debugger starts if STIN is found high. STIN has a built-in pull-down. It should be grounded or left open for normal operation.

STOUT	86	Out	33	Serial test output. 57.6 kbauds async output used for firmware debugging.
MIDI_OUT2	86	Out	33	Additional serial MIDI out
PDWN/	96	In Pu	-	Power down, active low. When power down is active, WCS0/, WCS1/, WWE/, WOE/, MIDI_OUT, STOUT are output 1. Address and data lines are output 0. All other outputs are set to 0. The crystal oscillator is stopped and supply voltage is removed from the core. To exit from power down, PDWN/ must be set to VD33, then RESET/ applied. When unused this pin must be left open or connected to VD33.
TEST0, TEST1	95,99	In Pd	-	Test inputs. Should be grounded or left open.
NC	1,32,64,67,97, 98,105,128	-	-	Not connected pins. Should be grounded or left open.

4.2. Alternate functions quick view

4.2.1. Key table

	Host 8 bit // interface
	Serial Slave Synchronous interface
	LCD display
	NAND FLASH – 3 different allowed connections
	Clocks for digital audioIN slave mode: CLAD/WSAD commonly used by DAAD inputs
	DataFlash/EEPROM interface SD Card interface (if SPI mode 0 compatible)

4.2.2. Functions per pin

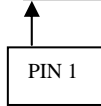
Pin Name Main Function	Alternate Function 1	Alternate Function 2	Alternate Function 3	Alternate Function 4
DEVICE INTERFACE				
DFSO				
DFSI				
DFSCK				
STIN				
STOUT	MIDI_OUT2			
MIDI_IN	SDIN			P0.14
MIDI_OUT				P0.9
CS	SYNC	ENB		P0.11
RD/		RS	NFR B/	P0.13
WR/		RW	NFWP/	P0.12
A0	SCLK		NFPRE	P0.10
IRQ	INT/		NFRE/	P0.8
D7 - D0		DB7 - DB0	I/O7 - I/O0	P0.7 - P0.0
CLAD - WSAD				P3.9 - P3.8
MEMORY INTERFACE				
WCS0/		XCS11/		
WCS1/				
WOE/				
WWE/				
WD15 - WD0	I/O15 - I/O0			P4.15 - P4.0
WA14 - WA0				
WA16 - WA15				P1.1 - P1.0
WA17	FS0			P1.2
WA18	FS1			P1.3
WA19	NFPRE			P1.4
WA20	NFWP/			P1.5
WA21	NFR B/			P1.6
WA22	NFRE/			P1.7
WA23	NFCLE		NFCLE	P1.8
WA24	NFWE/	XCS02/	NFWE/	P1.9
WA25	NFALE	XCS04/	NFALE	P1.10
WA26	NFCE/	XCS23/	NFCE/	P1.11
DIGITAL AUDIO IN/OUT				
CKOUT				
CLBD				
WSBD				
DABD0				
DABD1		NFWP/		P2.8
DABD2		NFR B/		P2.9
DABD3		NFRE/		P2.10
DABD4		NFCLE		P2.11
DABD5		NFWE/		P2.12
DABD6		NFALE		P2.13
DABD7		NFCE/		P2.14
DAAD0		I/O0		P2.0
DAAD3 - DAAD0		I/O3 - I/O0		P2.3 - P2.0
DAAD5 - DAAD4	CLADX2 - WSADX2	I/O5 - I/O4		P2.5 - P2.4
DAAD7 - DAAD6	CLADX1 - WSADX1	I/O7 - I/O6		P2.7 - P2.6

4.3. Pin-out by pin

Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name
1	NC	33	GND	65	CLAD	97	NC
2	WD9	34	WA17	66	WSAD	98	NC
3	WD10	35	WA18	67	NC	99	TEST1
4	WD11	36	WA19	68	D7	100	GND
5	GND	37	WA20	69	D6	101	X1
6	WD12	38	VM33	70	D5	102	X2
7	WD13	39	WA21	71	D4	103	LFT
8	WD14	40	WA22	72	D3	104	VD18
9	WD15	41	WA23	73	D2	105	NC
10	VREF	42	WA24	74	D1	106	GND
11	VM33	43	WA25	75	D0	107	VD33
12	GND	44	WA26	76	IRQ	108	GND
13	WA0	45	GND	77	VD33	109	VD33
14	WA1	46	OUTVC182	78	GND	110	OUTVC181
15	WA2	47	VD33	79	A0	111	GND
16	WA3	48	DABD1	80	WR/	112	WOE/
17	WA4	49	DABD2	81	RD/	113	WWE/
18	WA5	50	DABD3	82	CS/	114	VM33
19	WA6	51	DABD4	83	MIDI_IN	115	WCS0/
20	WA7	52	DABD5	84	MIDI_OUT	116	WCS1/
21	WA8	53	DABD6	85	STIN	117	WD0
22	WA9	54	GND	86	STOUT	118	WD1
23	GND	55	DABD7	87	CKOUT	119	GND
24	VM33	56	DAAD0	88	CLBD	120	WD2
25	WA10	57	DAAD1	89	WSBD	121	WD3
26	WA11	58	DAAD2	90	DABD0	122	WD4
27	WA12	59	DAAD3	91	DFSI	123	WD5
28	WA13	60	DAAD4	92	DFSO	124	WD6
29	WA14	61	DAAD5	93	DFCK	125	WD7
30	WA15	62	DAAD6	94	RESET/	126	WD8
31	WA16	63	DAAD7	95	TEST0	127	VM33
32	NC	64	NC	96	PDWN/	128	NC

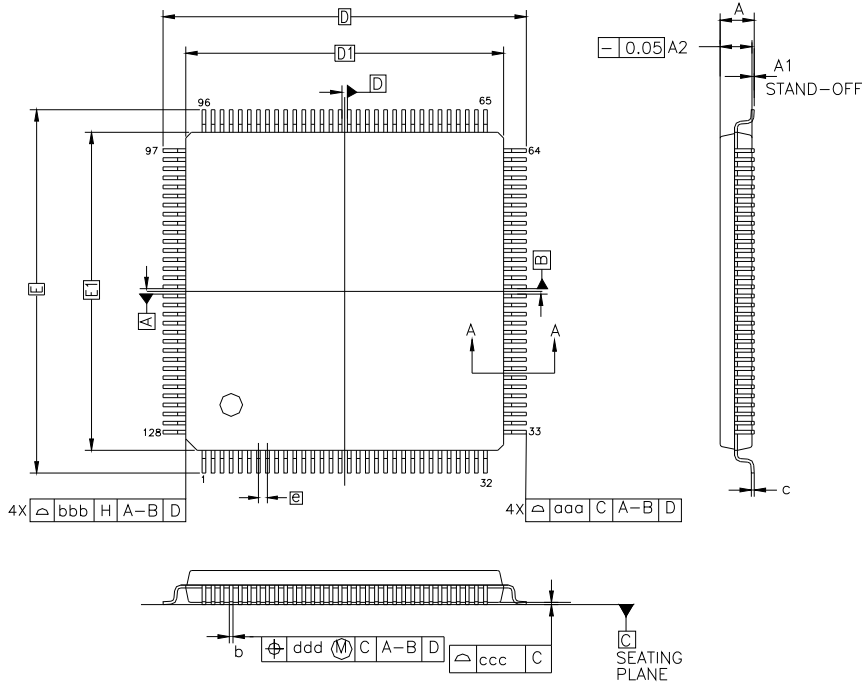
5. Marking

R-LQ128_G

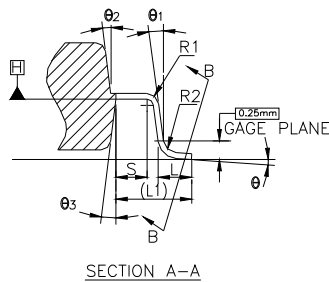
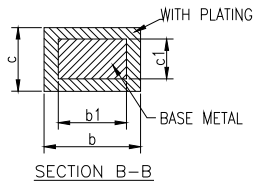


6. Mechanical dimensions

R-LQ128_G - LQFP



ALL DIMENSIONS ARE IN MILLIMETERS.



SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	16.00 BASIC			0.630 BASIC		
D1	14.00 BASIC			0.552 BASIC		
E	16.00 BASIC			0.630 BASIC		
E1	14.00 BASIC			0.552 BASIC		
R2	0.08	—	0.20	0.003	—	0.008
R1	0.08	—	—	0.003	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	—	—	0°	—	—
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°
c	0.09	—	0.20	0.004	—	0.008
c1	0.09	0.127	0.16	0.004	0.005	0.006
L1	1.00 REF			0.039 REF		
L	0.45	0.60	0.75	0.018	0.024	0.030
S	0.20	—	—	0.008	—	—
b	0.13	—	0.23	0.005	—	0.009
b1	0.13	0.16	0.19	0.005	0.006	0.007
e	0.40 BSC.			0.016 BSC.		
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.07			0.003		

	ZI 21140 Semur-en-Auxois FRANCE	TITLE Thin Quad Flat Pack (LQFP), 128 Pins	Package designation R-LQ128_G	REV. B
		Body : 14 x 14 x 1.4 mm Foot Print : 2 mm Pitch : 0.4 mm		

7. Electrical Characteristics

7.1. Absolute Maximum Ratings(*)

Parameter	Symbol	Min	Typ	Max	Unit
Temperature under bias	-	-55	-	+125	°C
Storage temperature	-	-65	-	+150	°C
Voltage on: X1 MEM pins, TEST0-1,PDWN/ 5VT pins	-	-0.3	-	VD18+.3	V
	-	-0.3	-	VD33+.3	V
	-	-0.3	-	5.5	V
Supply voltage	VD18	-0.3	-	1.95	V
	VD33	-0.3	-	3.6	V
	VM	-0.3	-	3.6	V
Maximum IOL per I/O pin (excepted MEM pins)	-	-	-	10	mA
Maximum IOH per I/O pin (excepted MEM pins)	-	-	-	10	mA
Maximum IOL per I/O MEM pin	-	-	-	10	mA
Maximum IOH per I/O MEM pin	-	-	-	10	mA

*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the Recommended Operating Conditions of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

7.2. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	VD18	1.65	1.8	1.95	V
Supply voltage	VD33	3	3.3	3.6	V
Operating ambient temperature	tA	0	-	70	°C

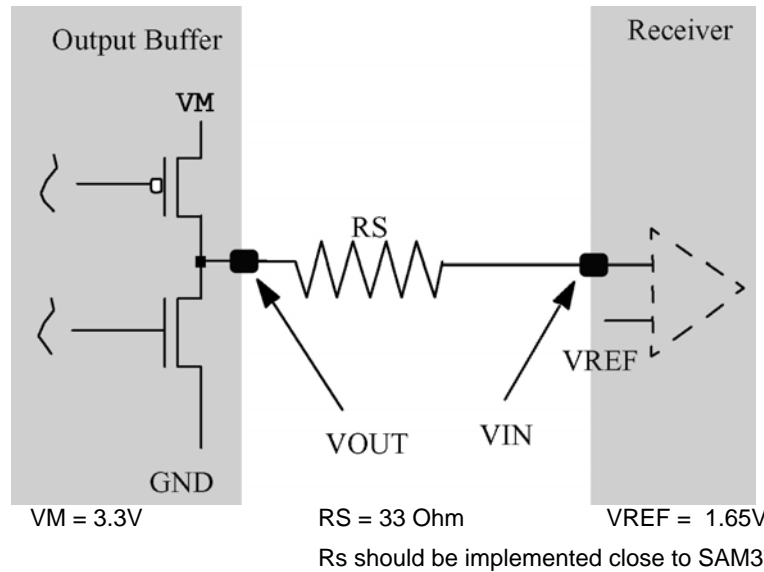
7.2.1. Memory pads

Memory pads (MEM) of SAM3716 are SSTL_2 and LVTTTL compliant.

Output drive of memory pads can be selected by firmware between Low (Class1) or High (Class 2).

Note

Default setting is High drive output. However it is recommended to switch to Low drive output for all standard applications with unterminated output load. High drive output should normally be never used.



Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	VM	2,3	3.3	3.6	V
Reference voltage	VREF	VM/2 - 0.04	1.65	VM/2 + 0.04	V
Serial resistor: Low drive output High drive output	RS	22	33	47	Ohm
	RS	68	82	100	Ohm

7.3. D.C. Characteristics (TA=25°C, VD18=1.8V±10%, VD33=3.3V±10%, VM33=3.3V±10%)

Parameter	Symbol	Min	Typ	Max	Unit
Low level input voltage: _{SVT} pads	VIL	-0.3	-	0.8	V
MEM pads	VIL	-0.3	-	0.8	V
TEST0-1, PDWN/	VIL	-0.3	-	0.8	V
High level input voltage: _{SVT} pads	VIH	2	-	5.5	V
MEM pads	VIH	2	-	3.6	V
TEST0-1, PDWN/	VIH	2	-	3.6	V
Low level output voltage: _{SVT} pads, IOL=8mA	VOL	-	-	0.4	V
MEM pads, IOL=8mA	VOL	-	-	0.4	V
High level output voltage: _{SVT} pads, IOH=8mA	VOH	VD33-0.4	-	-	V
MEM pads, IOH=8mA	VOH	VM-0.4	-	-	V
VD18 power supply current (crystal freq.=12.288 MHz, high speed PLL)	ID18	-	4	-	mA
VD33 power supply current (crystal freq. = 12.288 MHz, high speed PLL, all P24 stopped, warm Active Power-Down)	ID33	-	5.5	-	mA
VD33 deep power down supply current (PDWN/=0)	ID33	-	500	-	µA
VD33 power supply current (crystal freq.= 12.288 MHz, high speed PLL, all P24 stopped)	ID33	-	77	-	mA
VD33 power supply current (crystal freq.= 12.288 MHz, high speed PLL, all P24 running)	ID33	-	190	240	mA
VM power supply current (crystal freq.= 12.288 MHz, high speed PLL, all P24 stopped)	IDM	-	15	-	mA
VM power supply current (crystal freq.= 12.288 MHz, high speed PLL, all P24 running)	IDM	-	20	-	mA
Built-in pull-up / pull-down resistor	PU/PD	30	50-	100	kOhm

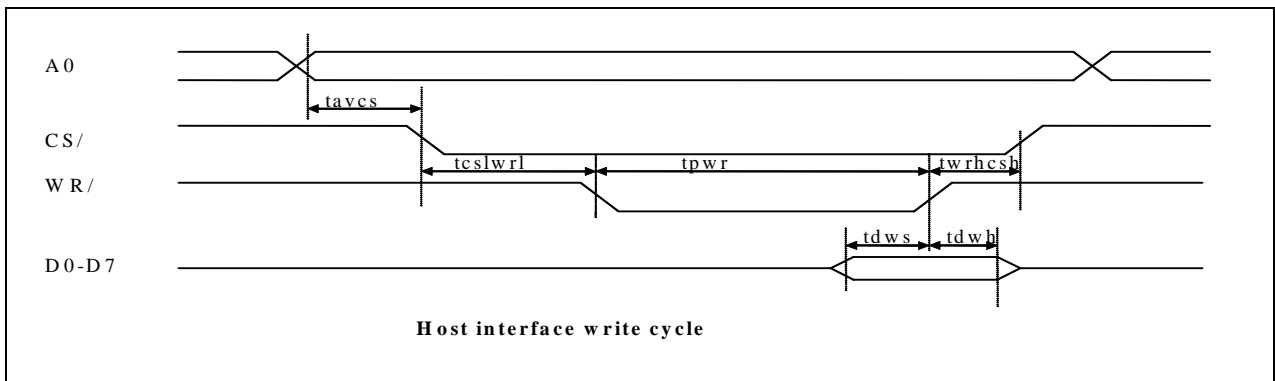
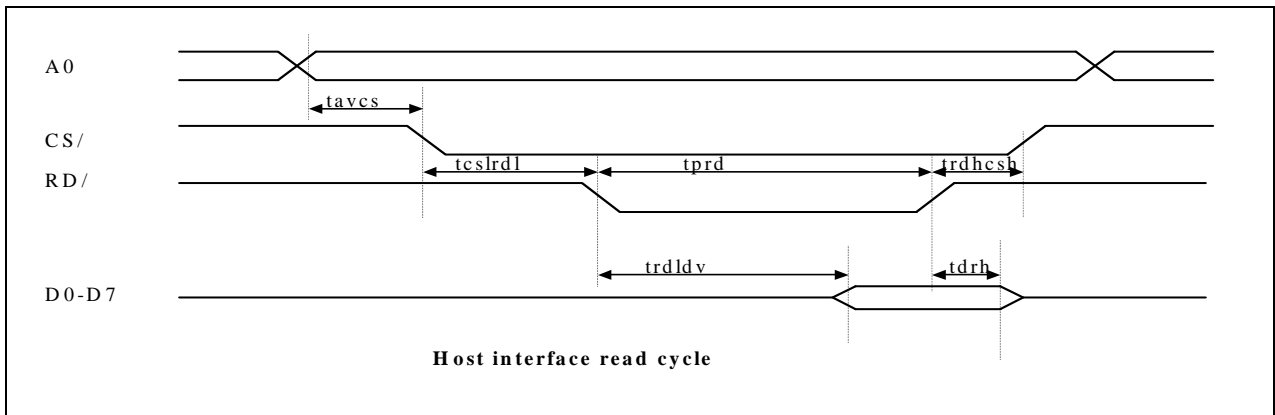
8. Peripherals and Timings

A built-in PLL multiplies the Xtal clock frequency by 4 or 6 for internal use. plck is the period of the internal clock generated by PLL. plck = tck/4 or tck/6. Typical values with Xtal 12.288 MHz are plck = 20 ns or 13.6 ns.

8.1. Slave 8bit parallel interface

Pins used: D7-D0 (I/O), CS/ (input), A0 (input), WR/ (input), RD/ (input), IRQ (output)
 This interface is typically used to connect the chip to a host processor.

- Timings



Parameter	Symbol	Min	Typ	Max	Unit
Address valid to chip select low	tavcs	0	-	-	ns
Chip select low to RD/ low	tcslrdl	0	-	-	ns
RD/ high to CS/ high	trdhcsh	0	-	-	ns
RD/ pulse width	tprd	plck	-	-	ns
Data out valid from RD/	trlddv	-	-	5	ns
Data out hold from RD/	tdrh	0	-	5	ns
Chip select low to WR/ low	tcslwrl	0	-	-	ns
WR/ high to CS/ high	twrhcsh	0	-	-	ns
WR/ pulse width	tpwr	plck	-	-	ns
Write data setup time	tdws	10	-	-	ns
Write data hold time	tdwh	0.9	-	-	ns

- IO Status Register

TE	RF	X	X	ID3	ID2	ID1	ID0
----	----	---	---	-----	-----	-----	-----

Status register is read when A0 = 1, RD/ = 0, CS/ = 0

- **TE: Transmit Empty:** This bit is 1 when nothing is transmitted from SAM3716 to host. If 0, data from SAM3716 to host is pending and IRQ pin is high. Host reading the data with pin A0=0 sets TE to 1 and clear IRQ. TE bit is actually reflecting inverted value of IRQ pin (IRQ/).

- **RF: Receiver Full:** Host should not write any data or control to SAM3716 if this bit is 1. When 0, then SAM3816 is ready to accept data from host.

- **ID[3:0]:** these 4 bits are firmware dependant and may be used for defining type of data sent by SAM3716 in case of multiple flows of data.

Host read should be performed with following steps:

- Nothing to read if IRQ pin is low. First wait for IRQ pin being high
- Read status (A0=1) to get ID[3:0] (this step is optional if ID[3:0] bits are not used and not defined by firmware)
- Read data (A0=0) (IRQ goes low at the end of read cycle, on rising edge of RD/ signal)
- Wait for IRQ pin being high again...

Note: On steps a) and d), if IRQ pin is not connected and not used, host can also read status and wait for TE bit=0

Host write should be done with following steps:

- Read status (A0=1). If bit RF=0, go to step b). If bit RF=1, read again status till bit RF going to 0.
- Write new data (A0=0) or new control (A0=1)

Note about step a):

There are two different cases for RF bit being 1:

- RF bit is 1 because FIFO of P16 is full. RF bit will go low again as soon as P16 is reading some bytes of the FIFO in order to have some free space again inside fifo and then is clearing bit 7 (FIFULL) of port 1 (CONTROL/STATUS). This time is firmware dependant.

- RF bit is 1 because previous host write has still not been written into the P16 FIFO. This case can happen if P16 is executing a long instruction. The writing will be indeed performed only when P16 has finished the instruction. Time for RF bit going low again in this case correspond to the longest P16 instruction which is max 12 us.

Consequently, if host write cycle time is always higher than 12 us, and if FIFO defined in firmware is big enough, host can be sure that RF bit will never be set. In such case, step a) can be bypassed by host.

8.2. NAND Flash and other peripheral interface

This is a master 8-bit or 16-bit parallel interface, allowing connection to NAND Flash or other peripherals such as LCD screens.

Pins used:
 I/O7-I/O0 or I/O15-I/O0 (I/O)
 NFPRE, NFCE/, NFALE, NFCLE, NFRE/, NFWE/ (outputs)

All these pins are fully under firmware control, therefore timing compatibility is ensured by firmware only.

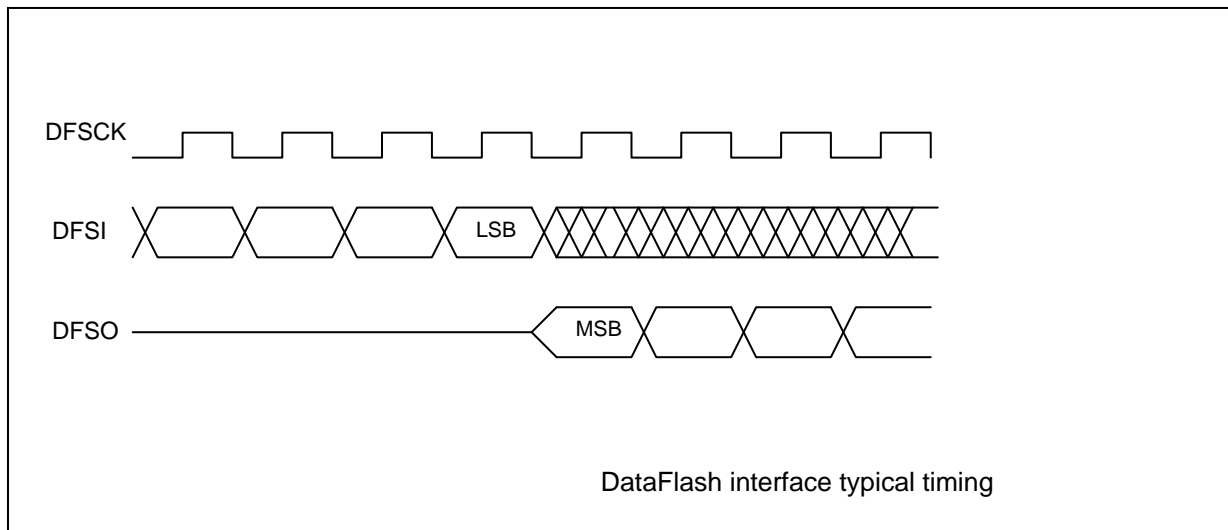
8.3. EEPROM / DataFlash interface

This is a master synchronous serial interface, operating in SPI mode 0.

Pins used:
 DFSI, DFSCK (outputs)
 DFSO (input)

The DFSCK frequency is firmware programmable from $f_{ck}/4$ to $f_{ck}/256$, f_{ck} being the system clock frequency ($f_{ck}=1/plck$). This allows accommodating a large variety of EEPROM/DataFlash devices.

Please refer to Atmel DataFlash datasheets for accurate SPI mode 0 timing.



8.4. Serial slave synchronous interface

The SAM3716 can be controlled by an external host processor through this unidirectional serial interface. However, no firmware can be downloaded at power-up through this interface.

Pins used:
 SCLK, SYNC, SDIN (input)
 INT/ (output)

Data is shifted MSB first. The IC samples an incoming SDIN bit on the rising edge of SCLK, therefore the host should change SDIN on the negative SCLK edge.

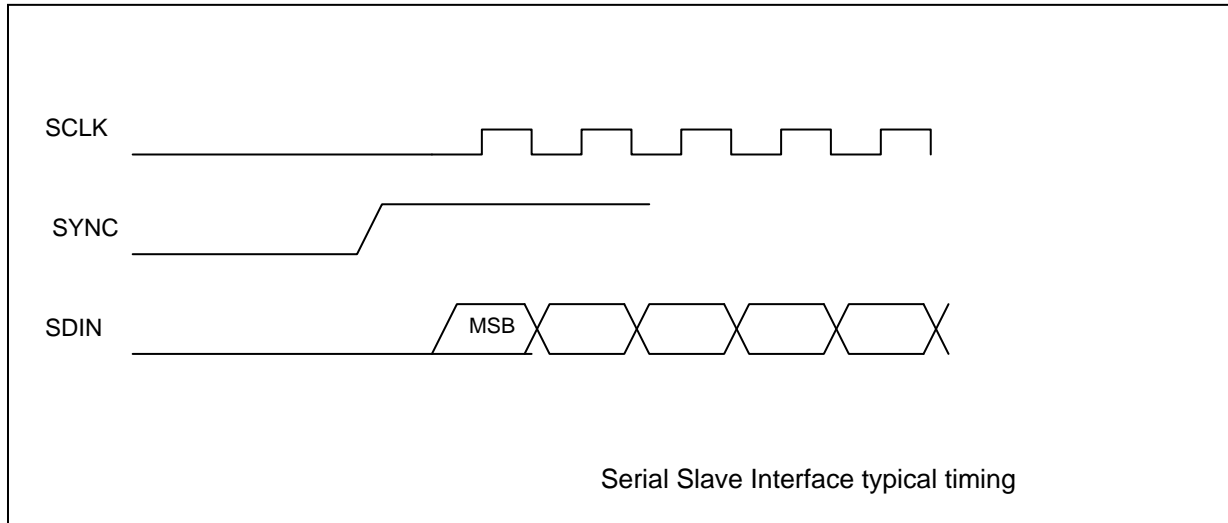
SYNC allows initial synchronization. The rising edge of SYNC, which should occur with SCLK low, indicates that SDIN will hold MSB data on the next rising SCLK.

The data is stored internally into a FIFO. Size of FIFO is firmware dependant. Minimum size is 128 bytes. Host should stop sending data as soon as INT/ goes high.

When the FIFO count is below 64, the INT/ output goes low. This allows the host processor to send data in burst mode.

The maximum SCLK frequency is $f_{ck}/4$ (f_{ck} being the system clock frequency. $f_{ck} = 1/plck$). The minimum time between two bytes is $256 plck$.

The contents of the SDIN data are defined by the firmware.



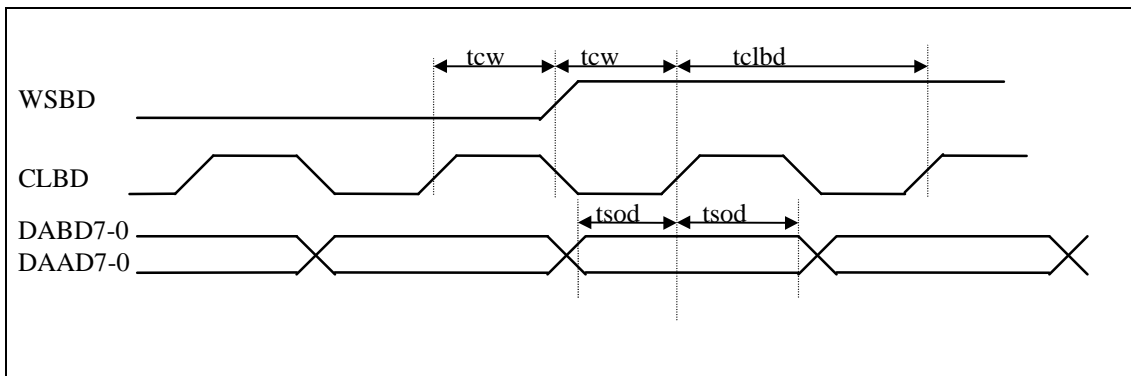
8.5. Digital audio

Pins used:
 CLBD, WSBD (outputs)
 DABD7-0 (outputs)
 DAAD7-0 (inputs)

And optionally
 CLAD, WSAD (inputs)

The SAM3716 allows for 16 digital audio output channels and 16 digital audio input channels. All audio channels are normally synchronized on single clocks CLBD, WSBD which are derived from the IC crystal oscillator. However, as a firmware option, the DAAD7-0 inputs can be individually synchronized with incoming CLAD and WSAD signals. In this case, the incoming sampling frequencies must be lower or equal to the chip sampling frequency.

The digital audio timing follows the I2S or MSB left standard, with up to 24 bits per sample



Parameter	Symbol	Min	Typ	Max	Unit
CLBD rising to WSBD change	tcw	tc-10	-	-	ns
DABD valid prior/after CLBD rising	tsod	tc-10	-	-	ns
CLBD cycle time	tclbd	-	2*tc	-	ns

tc is related to plck as follows:

Sample freq WSBD	tc	CLBD/WSBD freq ratio
1/(plck*512)	4*plck	64
1/(plck*768)	8*plck	48
1/(plck*1024)	8*plck	64
1/(plck*1536)	16*plck	48

Frame Format (FMT) is the number of plck cycles per digital audio frame. FMT is configurable by firmware. Possible values are: 512, 768, 1024, 1536

The choice of clock factors is done by the firmware. plck factor can have two values (see note below). Speed option allows single or double speed mode for CKOUT. As an example, table below show all possible clock combinations with 12.288MHz Xtal.

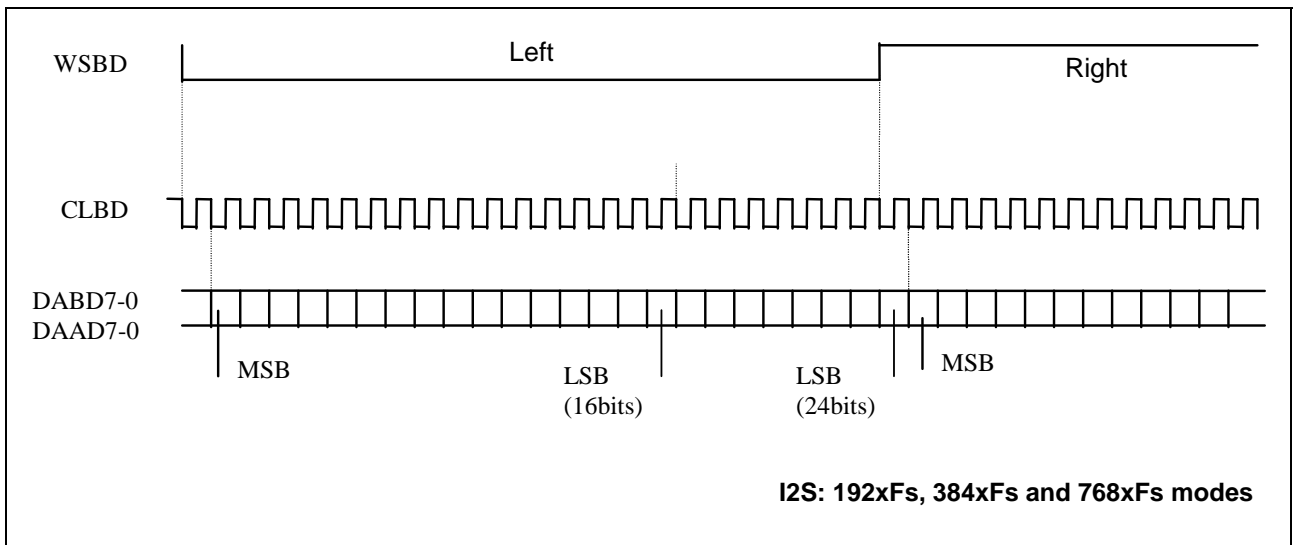
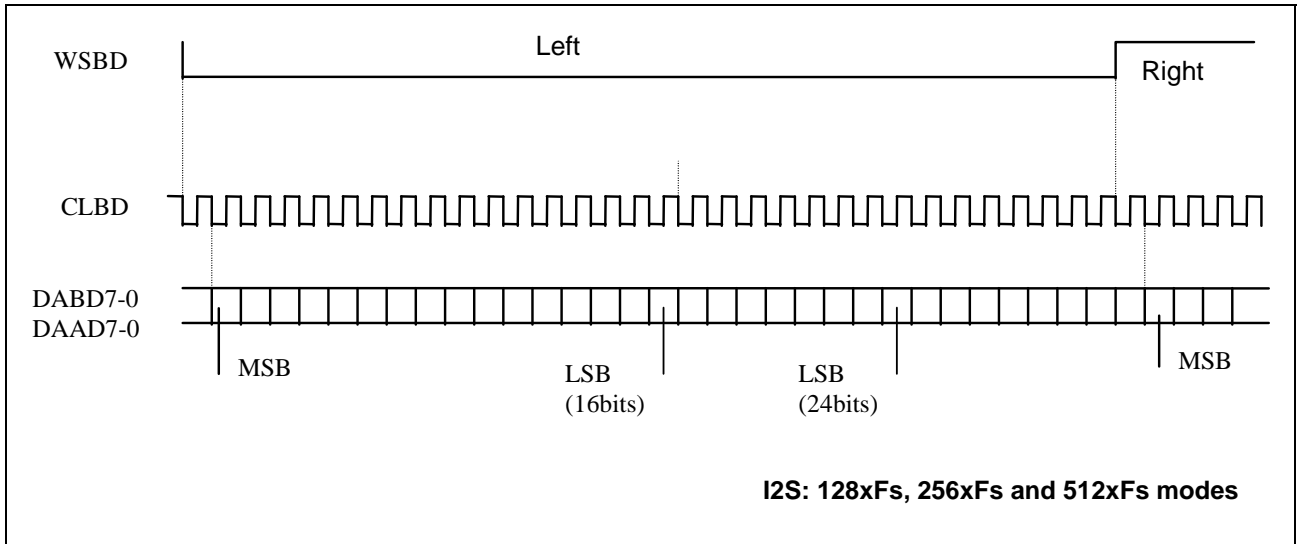
plck value	CKOUT Speed	FMT	CKOUT/WSBD freq ratio	CLBD/WSBD freq ratio	fs @ Xtal=12.288MHz
tck/4	Single	1536	384	48	32kHz
tck/4	Single	1024	256	64	48kHz
tck/4	Single	768	192	48	64kHz
tck/4	Single	512	128	64	96kHz
tck/4	Double	1536	768	48	32kHz
tck/4	Double	1024	512	64	48kHz
tck/4	Double	768	384	48	64kHz
tck/4	Double	512	256	64	96kHz
tck/6	Single	1536	384	48	48kHz (default)
tck/6	Single	1024	256	64	72kHz
tck/6	Single	768	192	48	96kHz
tck/6	Single	512	128	64	144kHz
tck/6	Double	1536	768	48	48kHz
tck/6	Double	1024	512	64	72kHz
tck/6	Double	768	384	48	96kHz
tck/6	Double	512	256	64	144kHz

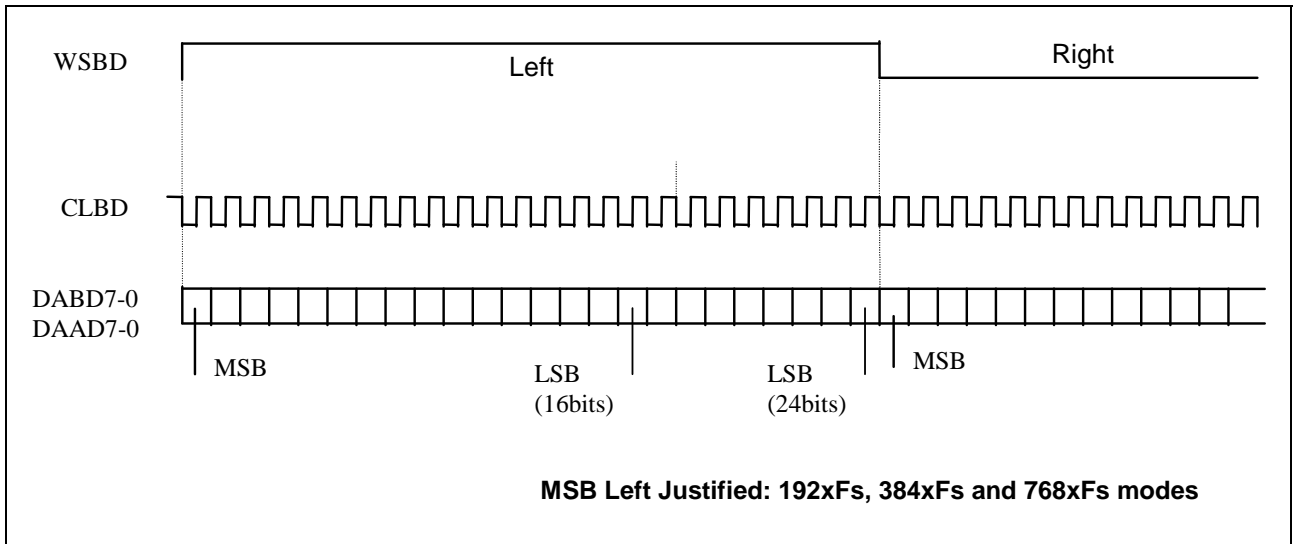
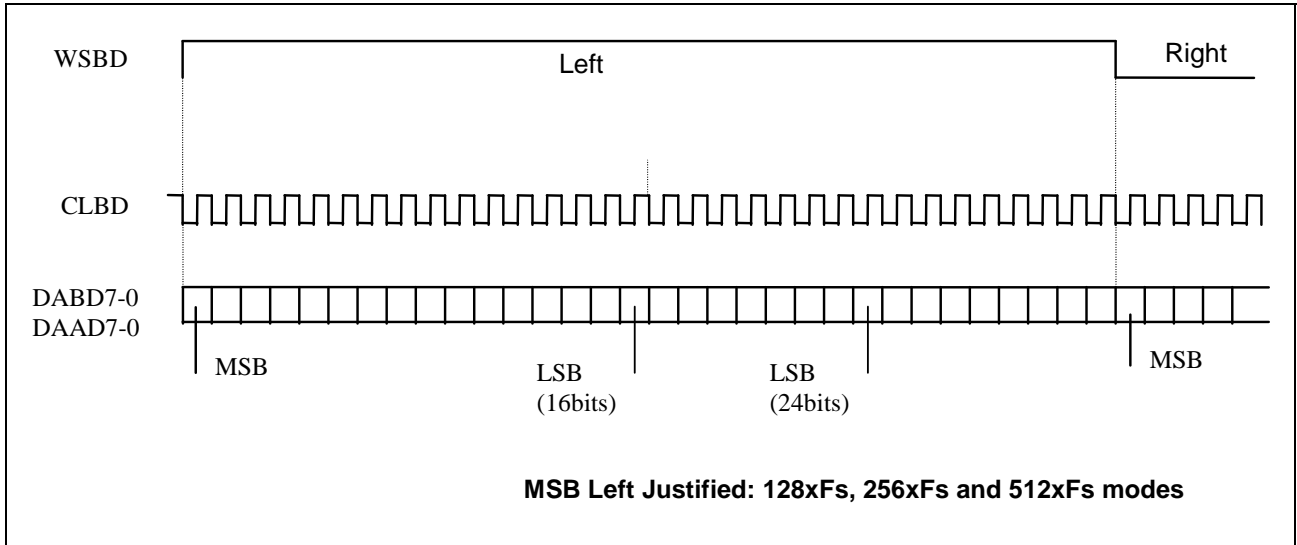
Note: For use with standard DREAM firmware/library only plck value = tck/6 can be used, with FMT=3 (48KHz).

CKOUT speed can be single or double, defined by firmware

DIGITAL AUDIO FRAME FORMAT

SAM3716 can generate I2S or MSB Left justified digital audio format. Master Clock CLBD can be 128x F_s , 256x F_s , 512x F_s , 192x F_s , 384x F_s or 768x F_s . Format and clock ratio are selected by firmware.





8.6. Serial MIDI_IN and MIDI_OUT

The serial MIDI IN and OUT signals are asynchronous signals following the MIDI transmission standard:

baud rate: programmable, typically 31.25 kb/s
 format: start bit(0), 8 data bits, stop bit(1)

8.7. External memory

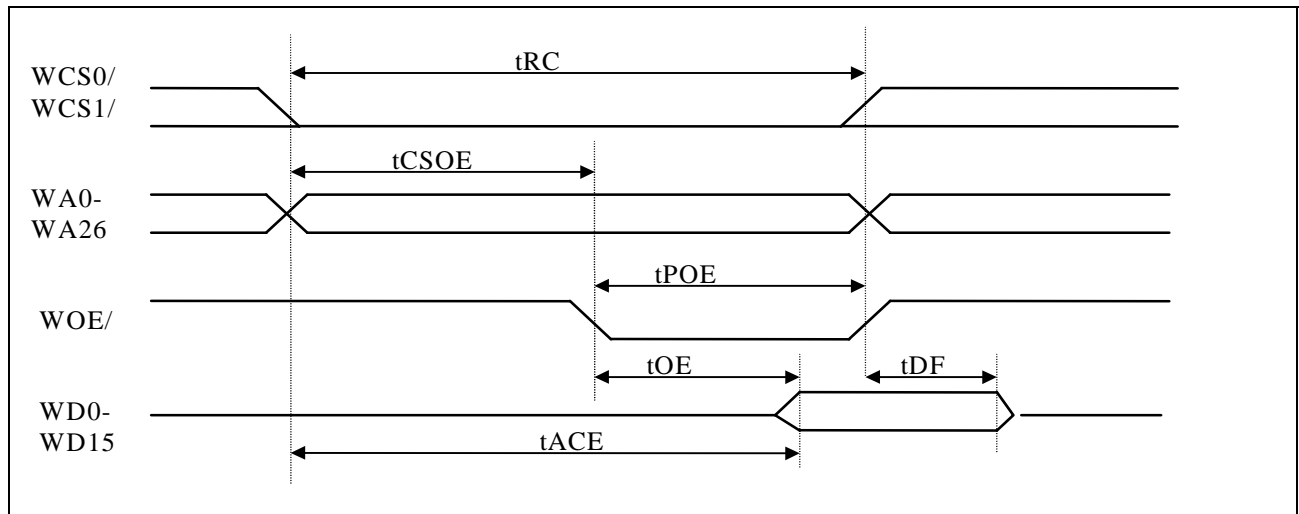
Pins used:

WA26-WA0: address out
 WD15-WD0: data bi-directional
 WCS0/ or XCS11/, XCS23/, XCS02/, XCS04/
 WCS1/

WOE/: output enable
 WWE/: write

When using all address bits, the maximum addressing range is two pages (WCS0/, WCS1/) of 128M words (total = 512 Mbytes).

ROM/Flash READ CYCLE

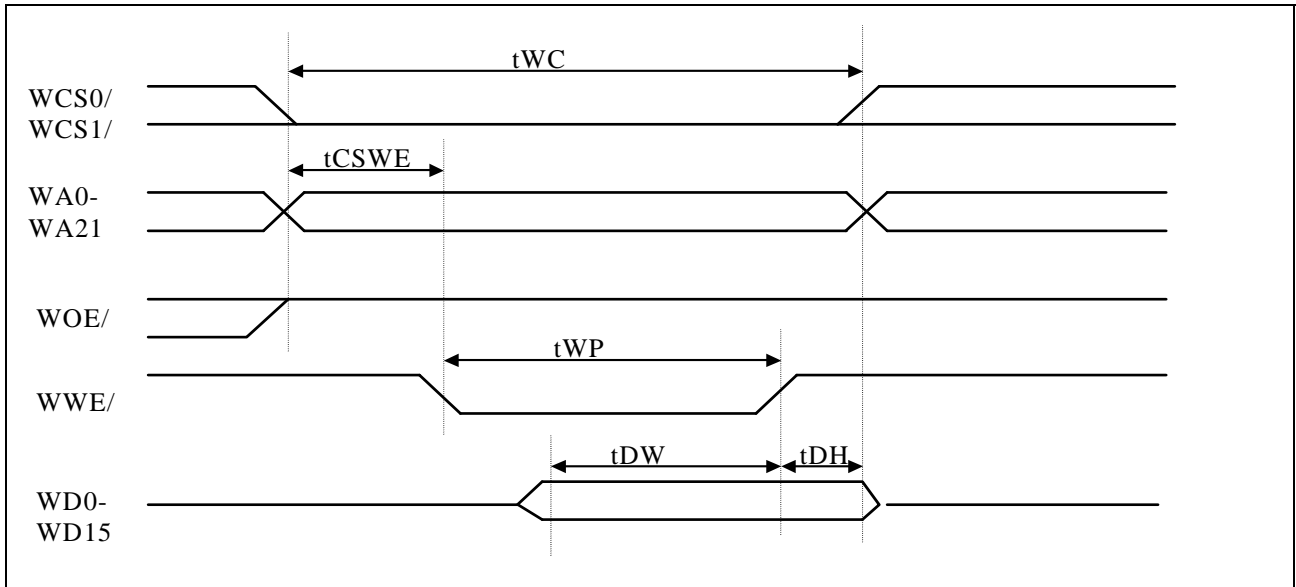


Parameter	Symbol	Min	Typ	Max	Unit
Read cycle time	tRC	N*plck-5	N*plck	N*plck+5	ns
Chip select low / address valid to WOE/ low	tCSOE	1*plck-5	1*plck	1*plck+5	ns
Output enable pulse width	tPOE	(N-1)*plck-5	(N-1)*plck	(N-1)*plck+5	ns
Chip select/address access time	tACE	(N-0.5)*plck-5	-	-	ns
Output enable access time	tOE	(N-1,5)*plck-5	-	-	ns
Chip select or WOE/ high to input data Hi-Z	tDF	0	-	1*plck	ns

Notes:

- N is number of system clock cycles. It can be programmed by firmware from 1 to 8
- Memory access time should be lower than tACEmin.

EXTERNAL RAM/FLASH WRITE TIMING



Parameter	Symbol	Min	Typ	Max	Unit
Write cycle time	t_{WC}	$N \cdot \text{plck} - 5$	$N \cdot \text{plck}$	$N \cdot \text{plck} + 5$	ns
Write enable low from CS/ or Address or WOE/	t_{CSWE}	$1 \cdot \text{plck} - 5$	$1 \cdot \text{plck}$	$1 \cdot \text{plck} + 5$	ns
Write pulse width	t_{WP}	$(N - 1) \cdot \text{plck} - 5$	$(N - 1) \cdot \text{plck}$	$(N - 1) \cdot \text{plck} + 5$	ns
Data out setup time	t_{DW}	$(N - 1) \cdot \text{plck} - 5$	-	-	ns
Data out hold time	t_{DH}	$0.5 \cdot \text{plck} - 5$	$0.5 \cdot \text{plck}$	$0.5 \cdot \text{plck} + 5$	ns

9. Reset and Power Down

During power-up, the RESET/ input should be held low until the crystal oscillator and PLL are stabilized, which takes max. 10ms.

After the low to high transition of RESET/, following happens:

- All P24s enter an idle state.
- P16 program execution starts in built-in ROM.

The power-up sequence is as follows:

- STIN is sensed. If HIGH, then the built-in debugger is started.
- Addresses 0 & 1 from internal Flash are checked. If "DR" is read, then control is transferred to address 400H from internal Flash.
- Firmware download from an host processor is assumed. (Download in 32k x 24 internal RAM)
 1. The byte 0ACh is written to the host, this rises IRQ. The host can recognize that the chip is ready to accept program download.
 2. The host sends the firmware size (in words) on two bytes (Low byte first).
 3. The host sends the SAM3716 firmware. The firmware should begin with string "DR".
 4. The byte 0ACh is written to the host, this rises IRQ. The host can recognize that the chip has accepted the firmware.
 5. SAM3716 starts the firmware.

If PDWN/ is asserted low, then the crystal oscillator and PLL are stopped. The chip enters a deep power down sleep mode, as power is removed from the core. To exit power down, PDWN/ has to be asserted high, then RESET/ applied.

Other power reduction features allowing warm restart are controlled by firmware:

- P24s can be individually stopped
- The clock frequency can be internally divided by 256

10. Recommended Board Layout

Like all HCMOS high integration ICs, following simple rules of board layout is mandatory for reliable operations:

- GND, VD33, VM33, VD18 distribution, decoupling

All GND, VD33, VM33, VD18 pins should be connected. A GND plane is strongly recommended. The board GND, VD33, VM33 and VD18 distribution should be in grid form.

Recommended VD18 decoupling is 0.1 μ F at each VD18 pin of the IC with an additional 10 μ F decoupling close to the crystal. Minimum recommended VM33 decoupling is 0.1 μ F at each VM33 pin. VD33 requires a single 0.1 μ F decoupling.

- Crystal

The paths between the crystal, the crystal compensation capacitors and the IC should be short and shielded. The ground return from the compensation capacitors filter should be the GND plane from the IC.

- Busses

Parallel layout from D7-D0 and WA26-WA0/WD15-WD0 should be avoided. The D7-D0 bus is an asynchronous type bus. Even on short distances, it can induce pulses on WA26-WA0/WD15-WD0 which can corrupt address and/or data on these busses.

A ground plane should be implemented below the D7-D0 bus, which connects both to the host and to the IC GND.

A ground plane should be implemented below the WA26-WA0/WD15-WD0 bus, which connects both to the Flash and RAM grounds and to the IC.

11. Product development and debugging

Dream provides an integrated product development and debugging tool SamVS. SamVS runs under Windows (98, ME, 2000, XP, Vista). Within the environment, it is possible to:

- Edit
- Assemble
- Debug on real target (In Circuit Emulation)
- Program internal or external Flash, NAND Flash; DataFlash, EEPROM on target.

Two dedicated IC pins, STIN and STOUT allow running firmware directly into the target using standard PC COM port communication at 57.6 kbauds. Thus time to market is optimized by testing directly on the final prototype.

A library of frequently used functions is available such as:

- Reverb
- Chorus
- Delay
- Compressor
- Pitch shifter
- Distortion
- Flanger
- Phaser
- Vocoder
- Feedback canceller
- MP3 decode
- 31 band equalizer
- Parametric equalizer

Dream engineers are available to study customer specific applications.

Dream Contact

info@dream.fr

Website

<http://www.dream.fr>

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